DETAILED ACTION

In view of the Appeal Brief filed on 03/22/2010, PROSECUTION IS HEREBY REOPENED.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181

Therefore the FINALITY of the office action dated 08/11/2009 is hereby withdrawn.

I. INTERVIEW SUMMARY

The interview mainly focused on getting a clear understanding of the core novelty of the instant invention, wherein the attorney presented a real world example of the instant invention as following: transferring buffered data via a single request as data is first read from a first part of a first buffer in a plurality of buffers, then skipping data in a second part of the first buffer in the plurality of buffers to read data from subsequent buffers in the plurality of buffers, and then wrapping around the plurality of buffers to read the skipped data in the second part of the first buffer, as shown in applicant's Figure 4; wherein, applicant's invention transfer data more efficiently as data is

transferred utilizing the single request, rather than the conventional two requests (i.e. need a second request to read the skipped data in the second part of the first buffer).

II. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

Authorization for this examiner's amendment was given in a telephone interview with Matt Zigmant, having Reg. No. 44,005, on 08/02/2010. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

NOTE: The claims amended by this examiner's amendment have been referred to by their original claim number and, if renumbered at time of allowance, also by the new number located in parentheses as required by **MPEP § 1302.04(g)**.

As per claim 1, claim 1 is replaced with -A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;

a memory interface, for connection to a memory device over a memory bus;

a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request, each of the plurality of buffers further including a plurality of sub-buffers; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality of buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer,

wherein, for a wrapping memory access request requiring multiple buffers <u>of the plurality of buffers</u>, data required for each of a beginning and an end of the wrapping

memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, the a beginning data and an end data for the wrapping memory access request being stored concurrently from a single data burst in the respective sub-buffers of the single respective buffer by the memory interface, the storing of the beginning and end data in the single respective buffer avoiding the need for an additional data burst to obtain the end data,

wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer, and

wherein when accessing the single respective buffer comprising a first part and a second part to return data to the respective device from which a wrapping memory read request requiring multiple data bursts over the memory bus was received, the beginning data is read out from the first part of the single respective buffer, the second part of the single respective buffer is skipped to read out subsequent data from at least one other of said multiple buffers, and the multiple buffers are wrapped around to read out the end data from the second part of the single respective buffer-.

As per claim 2, claim 2 is now cancelled.

As per claim 7 (currently renumbered as claim 6), claim 7 is replaced with -In a memory controller including at least one bus interface for connection to at least one

respective device for receiving memory access requests, a memory interface for connection to a memory device over a memory bus, a plurality of buffers in the memory interface, and control logic for placing received memory access requests into a queue of memory access requests, a method of retrieving data comprising:

in response to a received memory access request requiring multiple data bursts over the memory bus, assigning each of the multiple data bursts to a respective buffer in the plurality of buffers in the memory interface, each of the plurality of buffers being sized to store a data burst for the memory access request, each of the plurality of buffers further including a plurality of sub-buffers;

storing data from each of said multiple data bursts in the respective buffer in the memory interface;

for a wrapping memory access request requiring multiple buffers of the plurality of buffers, assigning data required for a beginning and an end of the wrapping memory access request to respective sub-buffers of a single respective buffer to be stored concurrently from a single data burst in the respective sub-buffers of the single respective buffer in the memory interface, the storing of a beginning data and an end data in the single respective buffer avoiding the need for an additional data burst to obtain the end data;

recording a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data; and

using the pointer to return to the indicated first sub-buffer to retrieve the end data,

wherein when accessing the single respective buffer comprising a first part and a second part to return data to the respective device from which a wrapping memory access request requiring multiple data bursts over the memory bus was received, the beginning data is read out from the first part of the single respective buffer, the end data is not read out from the second part of the single respective buffer, then data is read out from at least one other of said buffers, and then the multiple buffers are wrapped around and the end data is read out from the second part of the single respective buffer-.

As per claim 8, claim 8 is now cancelled.

As per claim 13 (currently renumbered as claim 11), claim 13 is replaced with -A programmable logic device, wherein the programmable logic device includes a memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device formed within the programmable logic device for receiving memory access requests;

a memory interface, for connection to an external memory device over a memory bus;

a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request, each of the plurality of buffers further including a plurality of sub-buffers; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality of buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer,

wherein, for a wrapping memory access request requiring multiple buffers of the plurality of buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, a beginning data and an end data for the wrapping memory access request being stored concurrently from a single data burst in the respective sub-buffers by the memory interface, the storing of the beginning and end data in the single respective buffer avoiding the need for an additional data burst to obtain the end data; and

wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single buffer,

wherein when accessing the single respective buffer comprising a first part and a second part to return data to the respective device from which a wrapping memory read request requiring multiple data bursts over the memory bus was received, the beginning data is read out from the first part of the single respective buffer, the second part of the

single respective buffer is skipped to read out subsequent data from at least one other of said multiple buffers, and the multiple buffers are wrapped around to read out the end data from the second part of the single respective buffer-.

As per claim 18 (currently renumbered as claim 14), claim 18 is replaced with -A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one device for receiving memory access requests;

a memory interface, for connection to a memory device over a memory bus;

a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, for a wrapping memory access request requiring multiple buffers of the plurality of buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to sub-buffers of a single buffer by the control logic, and

wherein the control logic records a value of a pointer indicating a first sub-buffer of the single buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single buffer,

wherein when accessing the single respective buffer comprising a first part and a second part to return data to the respective device from which a wrapping memory

access request requiring multiple data bursts over the memory bus was received, the beginning data is read out from the first part of the single respective buffer, the end data is not read out from the second part of the single respective buffer, then data is read out from at least one other of said buffers, and then the multiple buffer are wrapped around and the end data is read out from the second part of the single respective buffer-.

As per claim 19, claim 19 is now cancelled.

As per new claim 22 (currently renumbered as claim 4), new claim 22 is added as following “The memory controller of claim 1 wherein each of the plurality of sub-buffers are sized to store a data beat of the data burst stored in one of the corresponding plurality of buffers”.

As per new claim 23 (currently renumbered as claim 5), new claim 23 is added as following “The memory controller of claim 22 wherein the end data required for the wrapping memory access request is cached in one or more of the respective sub-buffers until needed for transfer in response to the wrapping memory access request”.

As per new claim 24 (currently renumbered as claim 9), new claim 24 is added as following “The method of claim 7 wherein each of the plurality of sub-buffers are sized to store a data beat of the data burst stored in one of the corresponding plurality of buffers”.

As per new claim 25 (currently renumbered as claim 10), new claim 25 is added as following "The method of claim 24 wherein the end data required for the wrapping memory access request is cached in one or more of the respective sub-buffers until needed for transfer in response to the wrapping memory access request"

As per new claim 26 (currently renumbered as claim 12), new claim 26 is added as following "The programmable logic device of claim 13 wherein each of the plurality of sub-buffers are sized to store a data beat of the data burst stored in one of the corresponding plurality of buffers".

As per new claim 27 (currently renumbered as claim 13), new claim 27 is added as following "The programmable logic device of claim 26 wherein the end data required for the wrapping memory access request is cached in one or more of the respective sub-buffers until needed for transfer in response to the wrapping memory access request".

III. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

Claims 1, 5-7, 11-13, 18 and 20-27 are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

The primary reason for allowance of independent claims 1 in the instant application is that the prior art of record, disclosed by the applicant and cited by the examiner, including the disclosures of Gray et al. (US Patent 6,816,923), Abramson et al. (US Patent 6,499,077), Iizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) neither anticipates nor renders obvious, alone or in combination, ***all*** the claimed limitations of independent claim 1. Because claims 5-6 and 22-23 (renumbered as claims 2-5 respectively) depend directly or indirectly on the independent claim 1, these claims are considered allowable for at least the same reasons noted above.

The primary reason for allowance of independent claims 7 (renumbered as claim 6) in the instant application is that the prior art of record, disclosed by the applicant and cited by the examiner, including the disclosures of Gray et al. (US Patent 6,816,923), Abramson et al. (US Patent 6,499,077), Iizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) neither anticipates nor renders obvious, alone or in combination, ***all*** the claimed limitations of independent claim 7 (renumbered as claim 6). Because claims 11-12 and 24-25 (renumbered as claims 7-10 respectively) depend directly or indirectly on the independent claim 7 (renumbered as claim 6), these claims are considered allowable for at least the same reasons noted above.

The primary reason for allowance of independent claims 13 (renumbered as claim 11) in the instant application is that the prior art of record, disclosed by the applicant and cited by the examiner, including the disclosures of Gray et al. (US Patent 6,816,923), Abramson et al. (US Patent 6,499,077), Iizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) neither anticipates nor renders obvious, alone or in combination, ***all*** the claimed limitations of independent claim 13 (renumbered as claim 11). Because claims 26-27 (renumbered as claims 12-13 respectively) depend directly or indirectly on the independent claim 13 (renumbered as claim 11), these claims are considered allowable for at least the same reasons noted above.

The primary reason for allowance of independent claims 18 (renumbered as claim 14) in the instant application is that the prior art of record, disclosed by the applicant and cited by the examiner, including the disclosures of Gray et al. (US Patent 6,816,923), Abramson et al. (US Patent 6,499,077), Iizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) neither anticipates nor renders obvious, alone or in combination, ***all*** the claimed limitations of independent claim 18 (renumbered as claim 14). Because claims 20-21(renumbered as claims 15-16 respectively) depend directly or indirectly on the independent claim 18 (renumbered as claim 14), these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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August 13, 2010

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